

IN THE CLAIMS:

Please cancel claims 25 and 26 without prejudice. Please add claims 27 and 28 as follows:

1 27. (New) A method of manufacturing a transistor comprising
2 a source and drain region and a channel region, the source and drain regions
3 being at least partially disposed in a bulk semiconductor substrate, the channel
4 region being disposed between the source and drain regions, the channel region
5 including a silicon germanium layer and a silicon cap layer, the method
6 comprising:

7 providing an amorphous semiconductor material including
8 germanium above a bulk substrate of semiconductor material;

9 providing an amorphous silicon layer above the amorphous
10 semiconductor material;

11 annealing the amorphous semiconductor material and the
12 amorphous silicon layer to form the silicon germanium layer and the silicon cap
13 layer, the silicon germanium layer and the silicon cap layer are single crystalline;
14 and

15 doping the single crystalline semiconductor layer and the substrate
16 at a source location and a drain location to form a source region and a drain
17 region, whereby the channel region between the source region and the drain
18 region includes at least a portion of the semiconductor germanium layer covered
19 by the silicon cap layer.